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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/061,544	02/01/2002	David C. Wyland	CRA-016	2708

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EXAMINER	
AUVE, GLENN ALLEN	
ART UNIT	**PAPER NUMBER**
2111	3

DATE MAILED: 05/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	10/061,544	WYLAND, DAVID C.	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 01 February 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. Applicant's IDS filed May 7, 2002, has been considered. However, it is not clear why the Wert et al. reference was cited as it appears to have no relevance at all to the present case.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Wenniger, U.S. Pat. No. 6,018,785.

As per claim 1, Wenniger shows a semaphore cell (abstract and throughout the specification); an interrupt generation circuit coupled to the semaphore cell (abstract and col.1, lines 32-40); a first processor coupled to the interrupt generation circuit (at least fig.3,(112)); wherein the semaphore cell is configured to have a first state and a second state, the first state of the semaphore cell indicating that a shared resource is available for access, and the second state of the semaphore cell indicating that the shared resource is unavailable for access (inherent in the operation of a semaphore and also in col.6), and the interrupt generation circuit is configured to generate a first semaphore interrupt signal to the first processor when the semaphore cell changes from the second state to the first state and when the first processor needs to access the shared resource (col.1 and col.6). Wenniger shows all of the elements recited in claim 1.

As for claim 2, the argument for claim 1 applies. Wenniger also shows that the interrupt generation circuit comprises a first semaphore interrupt enable cell coupled to the first processor and configured to have a third state and a fourth state, the third state of the first semaphore interrupt enable cell indicating that the first processor does not need to access the shared resource, and the fourth state of the first semaphore interrupt enable cell indicating that the first processor has read the semaphore cell and has determined that the semaphore cell is in the second state (fig.4 and cols. 6-8, wherein the interrupt is sent to the processor when the state of the semaphore changes). Wenniger shows all of the elements recited in claim 1.

As for claim 3, the argument for claim 2 applies. Wenniger also shows that the interrupt generation circuit further comprises a semaphore interrupt cell coupled to the semaphore cell and configured to have a fifth state and a sixth state, the sixth state of the semaphore interrupt cell indicating that the shared resource has just been made available for access (fig.4, and cols. 6-8). Wenniger shows all of the elements recited in claim 3.

As for claim 4, the argument for claim 3 applies. Wenniger also shows that the interrupt generation circuit further comprises a first gate coupled to the semaphore interrupt cell, the first semaphore interrupt enable cell, and the first processor, the first gate being configured to generate the first semaphore interrupt signal to the first processor if the first semaphore interrupt enable cell is in the fourth state and the semaphore interrupt cell is in the sixth state (fig.4, and cols. 6-8). Wenniger shows all of the elements recited in claim 4.

As for claim 5, the argument for claim 4 applies. Wenniger also shows that the first semaphore interrupt enable cell is further configured to change to the third state after the first semaphore interrupt signal is sent to the first processor (fig.4, and cols. 6-8). Wenniger shows all of the elements recited in claim 5.

As for claim 6, the argument for claim 4 applies. Wenniger also shows that the semaphore interrupt cell is further configured to change to the fifth state after the first semaphore interrupt signal is sent to the first processor (fig.4, and cols. 6-8). Wenniger shows all of the elements recited in claim 6.

As for claim 7, the argument for claim 4 applies. Wenniger also shows that the semaphore cell is configured to be in the second state after being read by any processor (fig.4, and cols. 6-8). Wenniger shows all of the elements recited in claim 7.

As for claim 8, the argument for claim 7 applies. Wenniger also shows that the semaphore cell comprises a flip-flop coupled to the first processor via a control line, the control line being used for transmitting both read/write signals and data to be stored in the flip-flop (fig.4, and cols. 6-8). Wenniger shows all of the elements recited in claim 8.

As for claim 9, the argument for claim 4 applies. Wenniger also shows that the interrupt generation circuit further comprises a second semaphore interrupt enable cell coupled to a second processor (114) and configured to have a seventh state and an eighth state, the seventh state of the second semaphore interrupt enable cell indicating that the second processor does not need to access the shared resource, and the eighth state of the second semaphore interrupt enable cell indicating that the second processor reads the semaphore cell and finds that the semaphore cell is in the second state (figs.4 and 7, and cols. 6-8). Wenniger shows all of the elements recited in claim 9.

As for claim 10, the argument for claim 9 applies. Wenniger also shows that the interrupt generation circuit further comprises a second gate coupled to the semaphore interrupt cell, the second semaphore interrupt enable cell, and the second processor, the second gate being configured to generate a second semaphore interrupt signal to the second processor if the second semaphore interrupt enable cell is in the eighth state and the semaphore interrupt cell is

in the sixth state (figs.4 and 7, and cols. 6-8). Wenniger shows all of the elements recited in claim 10.

As for claim 11, the argument for claim 10 applies. Wenniger also shows that the semaphore cell is configured to be in the second state after being read by any processor (figs.4 and 7, and cols. 6-8). Wenniger shows all of the elements recited in claim 11.

As for claim 12, the argument for claim 11 applies. Wenniger also shows that the semaphore cell comprises a flip-flop coupled to the first and second processors via a control line, the control line being used for transmitting both read/write signals and data to be stored in the flip-flop (figs.4 and 7, and cols. 6-8). Wenniger shows all of the elements recited in claim 12.

As per claim 13 Wenniger shows a method of using semaphores to monitor shared resource accesses (abstract and throughout the specification), the method comprising: providing a semaphore cell configured to have a first state and a second state, the first state of the semaphore cell indicating that a shared resource is available for access, and the second state of the semaphore cell indicating that the shared resource is unavailable for access; providing an interrupt generation circuit coupled to the semaphore cell; providing a first processor coupled to the interrupt generation circuit; and generating, with the interrupt generation circuit, a first semaphore interrupt signal to the first processor if the semaphore cell changes from the second state to the first state and if the first processor need to access the shared resource (all at least in cols.1 and 6-8 and figs. 3 and 4). Wenniger shows all of the steps recited in claim 13.

As for claim 14, the argument for claim 13 applies. Wenniger also shows that the step of generating, with the interrupt generation circuit, a first semaphore interrupt signal to the first processor comprises providing a first semaphore interrupt enable cell coupled to the first processor and configured to have a third state and a fourth state, the third state of the first

semaphore interrupt enable cell indicating that the first processor does not need to access the shared resource, and the fourth state of the first semaphore interrupt enable cell indicating that the first processor reads the semaphore cell and finds that the semaphore cell is in the second state (fig.4 and cols. 6-8, wherein the interrupt is sent to the processor when the state of the semaphore changes). Wenniger shows all of the elements recited in claim 14.

As for claim 15, the argument for claim 14 applies. Wenniger also shows that the step of generating, with the interrupt generation circuit, a first semaphore interrupt signal to the first processor further comprises providing a semaphore interrupt cell coupled to the semaphore cell and configured to have a fifth state and a sixth state, the sixth state of the semaphore interrupt cell indicating that the semaphore cell changes from the second state to the first state (fig.4 and cols. 6-8). Wenniger shows all of the elements recited in claim 15.

As for claim 16, the argument for claim 15 applies. Wenniger also shows that the step of generating, with the interrupt generation circuit, a first semaphore interrupt signal to the first processor further comprises: providing a first gate coupled to the semaphore interrupt cell, the first semaphore interrupt enable cell, and the first processor; and generating, with the first gate, the first semaphore interrupt signal to the first processor if the first semaphore interrupt enable cell is in the fourth state and the semaphore interrupt cell is in the sixth state (fig.4 and cols. 6-8). Wenniger shows all of the elements recited in claim 16.

As for claim 17, the argument for claim 16 applies. Wenniger also shows changing the first semaphore interrupt enable cell to the third state after the first semaphore interrupt signal is sent to the first processor (fig.4 and cols. 6-8). Wenniger shows all of the elements recited in claim 17.

As for claim 18, the argument for claim 16 applies. Wenniger also shows changing the semaphore interrupt cell to the fifth state after the first semaphore interrupt signal is sent to the first processor (fig.4 and cols. 6-8). Wenniger shows all of the elements recited in claim 18.

As for claim 19, the argument for claim 16 applies. Wenniger also shows that the step of providing the semaphore cell comprises providing a hardware semaphore cell (120). Wenniger shows all of the elements recited in claim 19.

As for claim 20, the argument for claim 19 applies. Wenniger also shows that the step of providing a hardware semaphore cell comprises providing a flip-flop coupled to the first processor via a control line, the control line being used for transmitting both read/write signals and data to be stored in the flip-flop (fig.4 and cols. 6-8). Wenniger shows all of the elements recited in claim 20.

As for claim 21, the argument for claim 16 applies. Wenniger also shows providing a second semaphore interrupt enable cell coupled to a second processor and configured to have a seventh state and an eighth state, the seventh state of the second semaphore interrupt enable cell indicating that the second processor does not need to access the shared resource, and the eighth state of the second semaphore interrupt enable cell indicating that the second processor reads the semaphore cell and finds that the semaphore cell is in the second state (fig.4 and 7, and cols. 6-8). Wenniger shows all of the elements recited in claim 21.

As for claim 22, the argument for claim 21 applies. Wenniger also shows providing a second gate coupled to the semaphore interrupt cell, the second semaphore interrupt enable cell, and the second processor; and generating, with the second gate, a second semaphore interrupt signal to the second processor if the second semaphore interrupt enable cell is in the eighth state and the semaphore interrupt cell is in the sixth state (fig.4 and 7, and cols. 6-8). Wenniger shows all of the elements recited in claim 22.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references cited but not applied show other semaphore systems.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (703) 305-9638. The examiner can normally be reached on M-Th 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
May 25, 2004